OIPE
JUN 07 2007
PATENT & TRADEMARK OFFICE

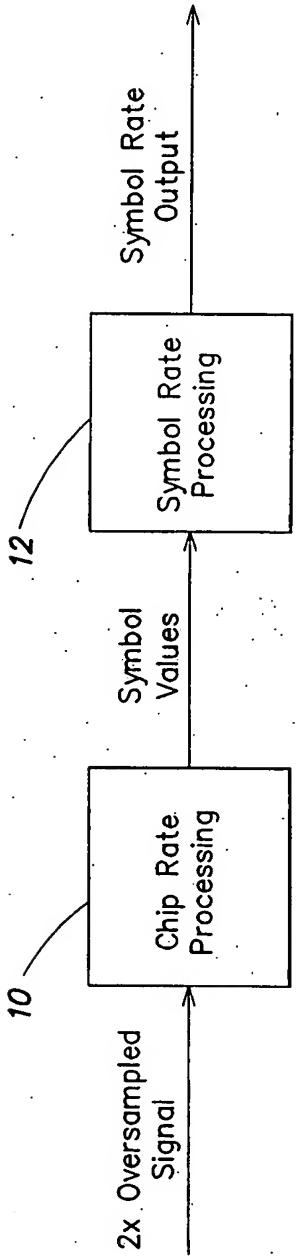

FIG. 1

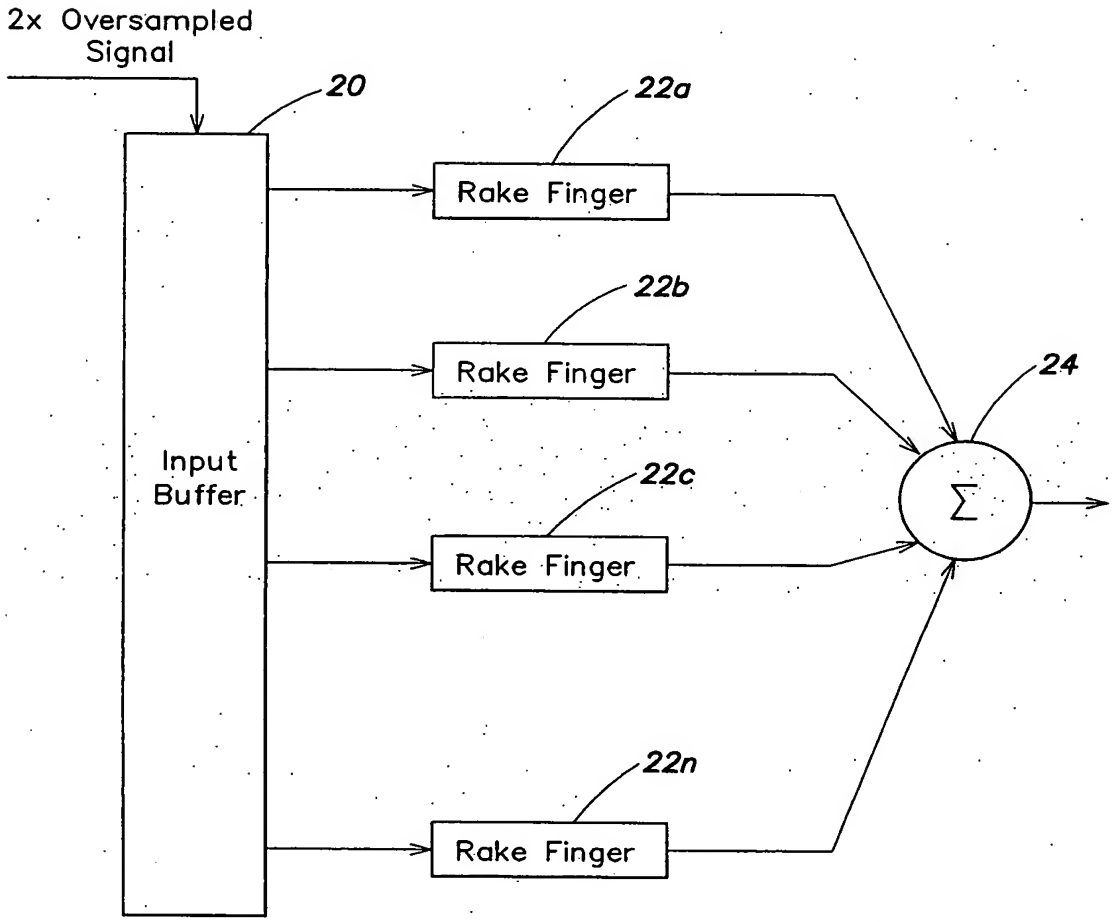
2x Oversampled Signal
20
22a
Rake Finger
22b
Rake Finger
24
Input Buffer
22c
Rake Finger
Σ
22n
Rake Finger

FIG. 2

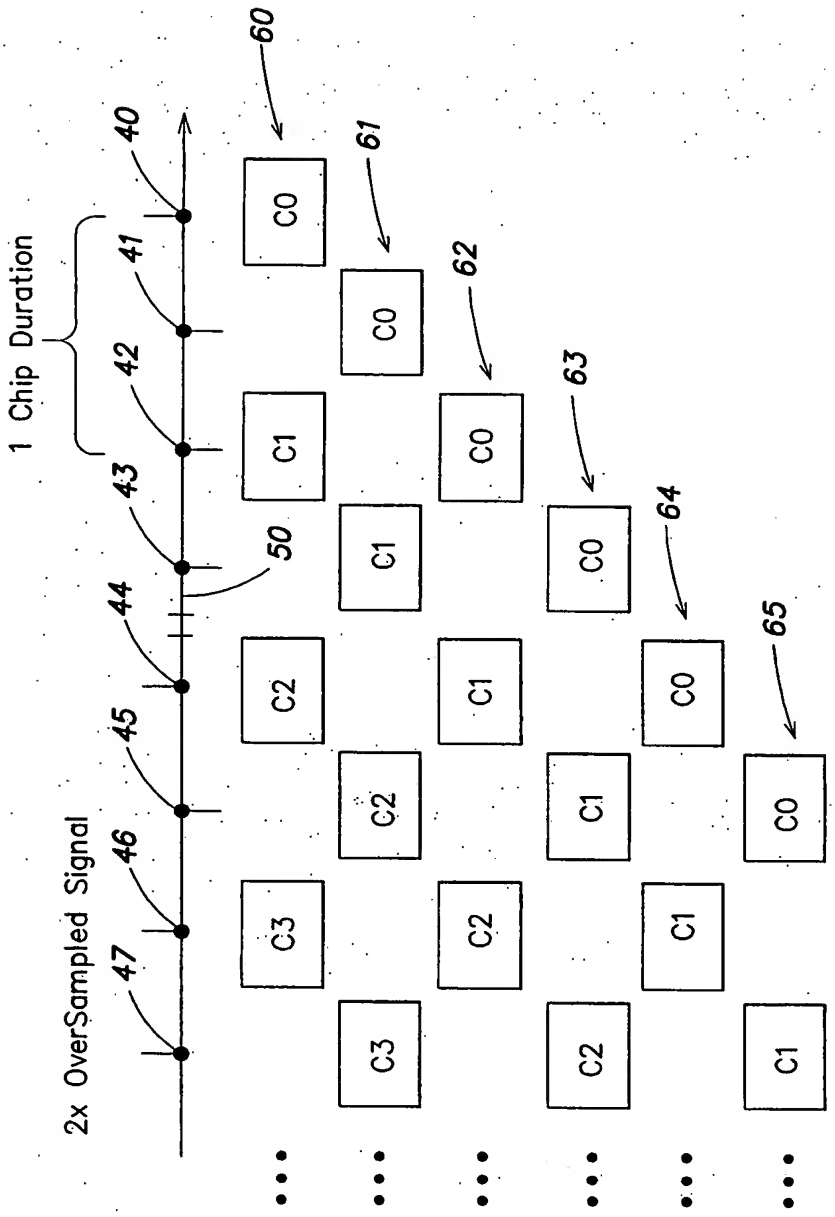
1 Chip Duration
2x OverSampled Signal
40
41
42
43
44
45
46
47
50
60
61
62
63
64
65
C0
C1
C2
C3

FIG. 3A

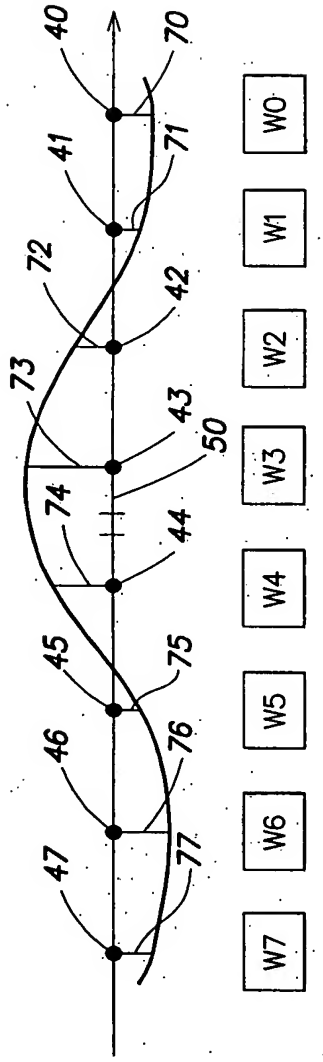
40
70
41
71
72
42
73
43
50
74
44
45
75
46
76
47
77
W0
W1
W2
W3
W4
W5
W6
W7

FIG. 3B

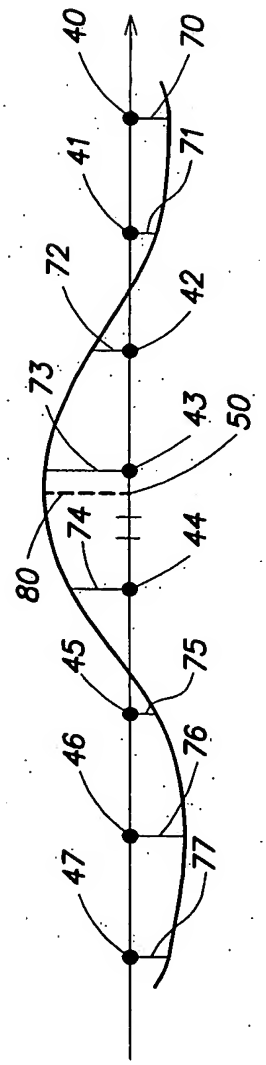
40
70
41
71
72
42
73
43
50
80
74
44
45
75
46
76
47
77

FIG. 3C

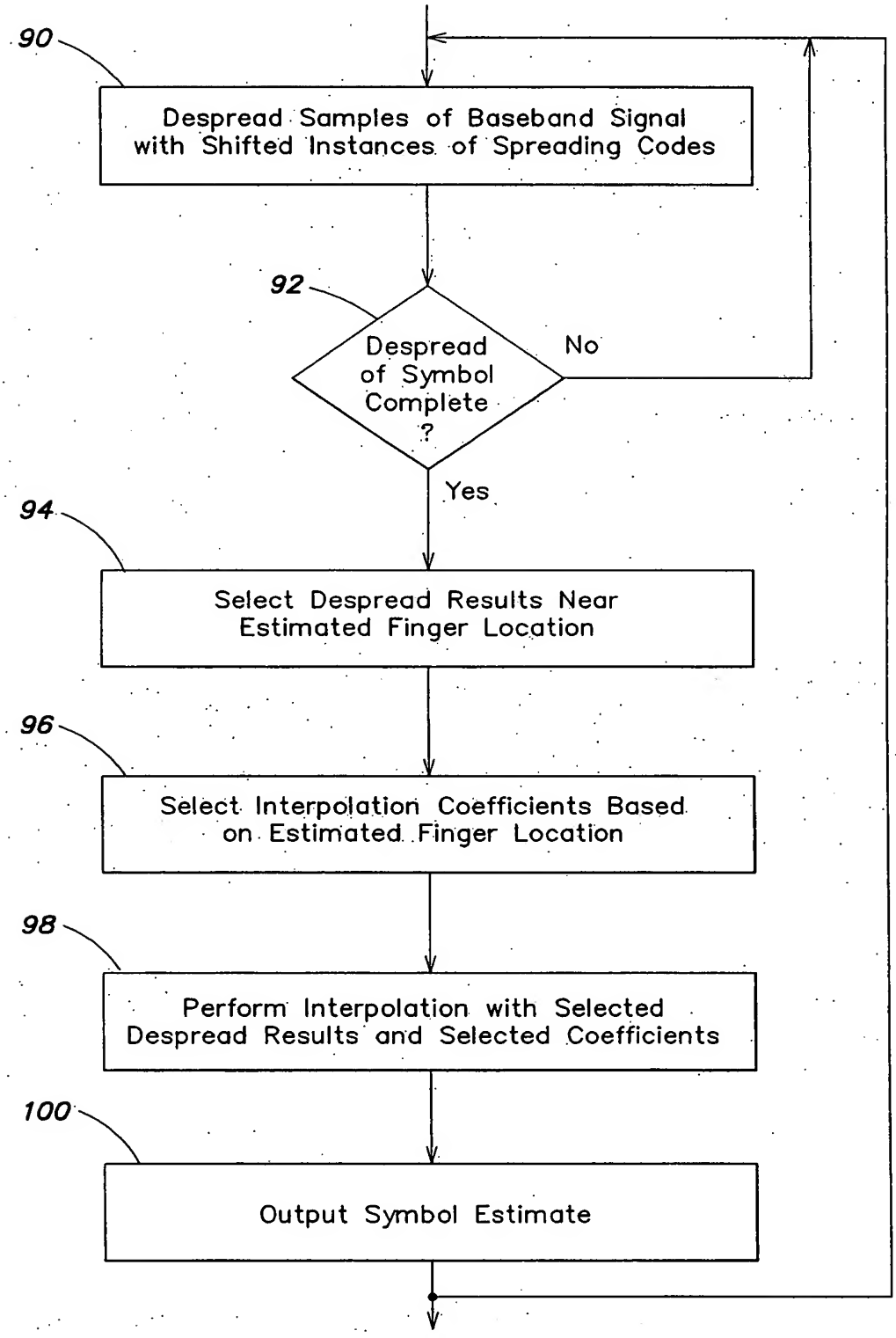
90
Despread Samples of Baseband Signal with Shifted Instances of Spreading Codes
92
Despread of Symbol Complete ?
No
Yes
94
Select Despread Results Near Estimated Finger Location
96
Select Interpolation Coefficients Based on Estimated Finger Location
98
Perform Interpolation with Selected Despread Results and Selected Coefficients
100
Output Symbol Estimate

FIG. 4

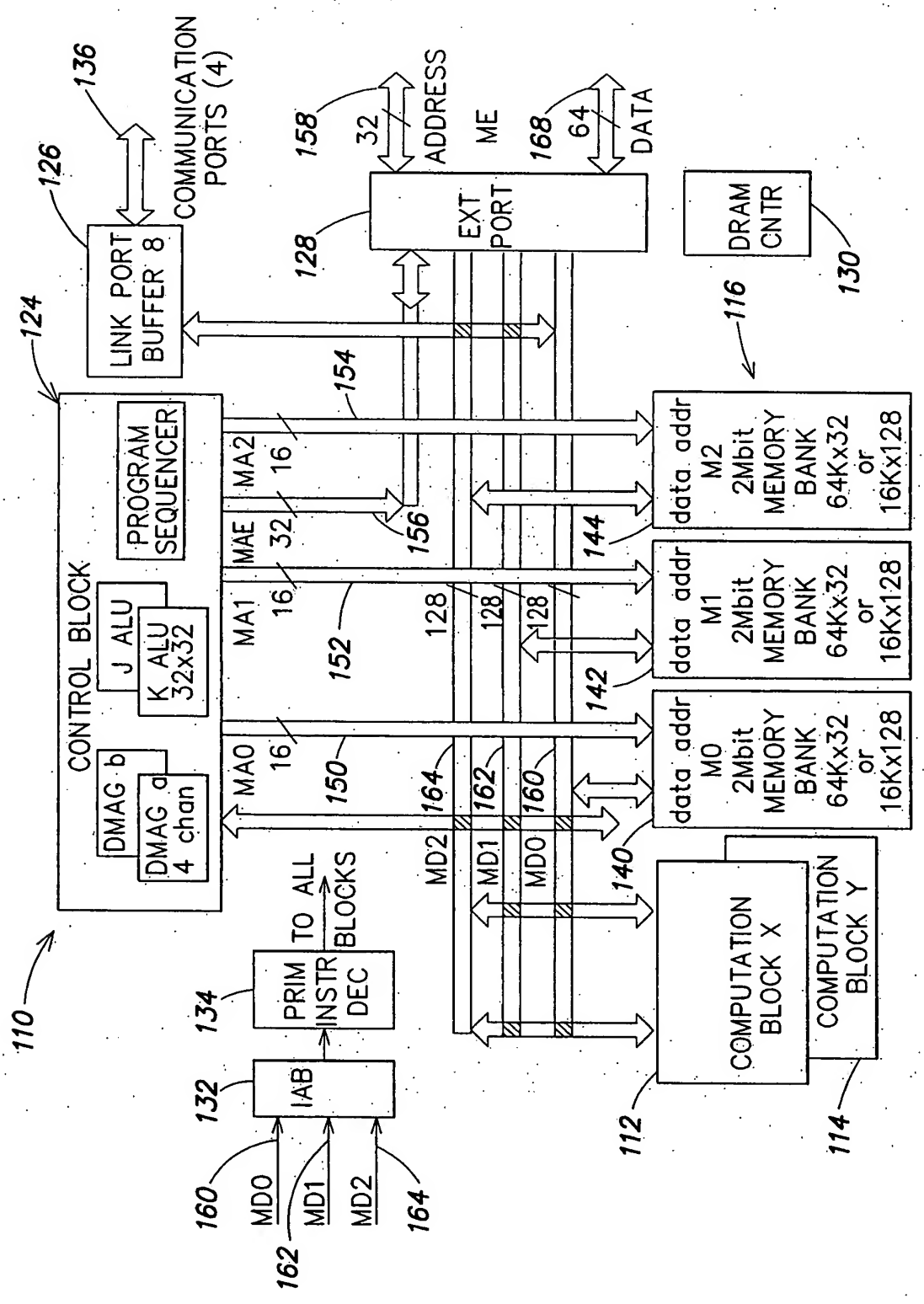
110
124
126
136
COMMUNICATION PORTS (4)
LINK PORT BUFFER 8
158
32
ADDRESS
ME
168
64
DATA
128
EXT PORT
DRAM CNTR
130
116
CONTROL BLOCK
PROGRAM SEQUENCER
J ALU
K ALU 32x32
DMAG b
DMAG a 4 chan
MA2
MAE
MA1
MA0
16
32
154
156
152
150
128
144
142
140
164
162
160
MD2
MD1
MD0
data addr M2 2Mbit MEMORY BANK 64Kx32 or 16Kx128
data addr M1 2Mbit MEMORY BANK 64Kx32 or 16Kx128
data addr M0 2Mbit MEMORY BANK 64Kx32 or 16Kx128
TO ALL BLOCKS
PRIM INSTR DEC
134
IAB
132
160
MD0
162
MD1
MD2
164
112
COMPUTATION BLOCK X
114
COMPUTATION BLOCK Y

FIG. 5

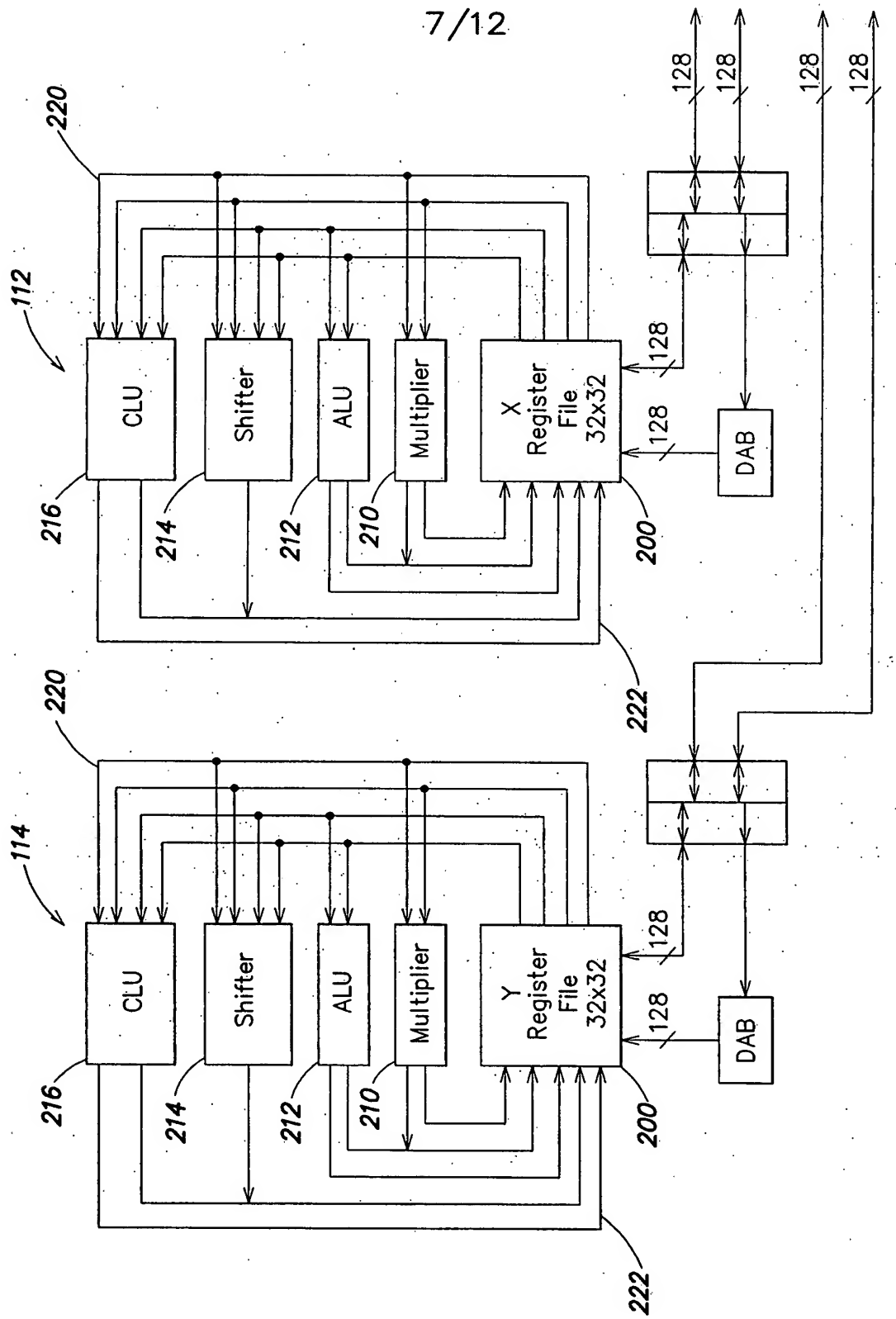
220
112
CLU
Shifter
ALU
Multiplier
X Register File 32x32
DAB
128
128
128
128
128
128
216
214
212
210
200
222
220
114
CLU
Shifter
ALU
Multiplier
Y Register File 32x32
DAB
128
128
216
214
212
210
200
222

FIG. 6

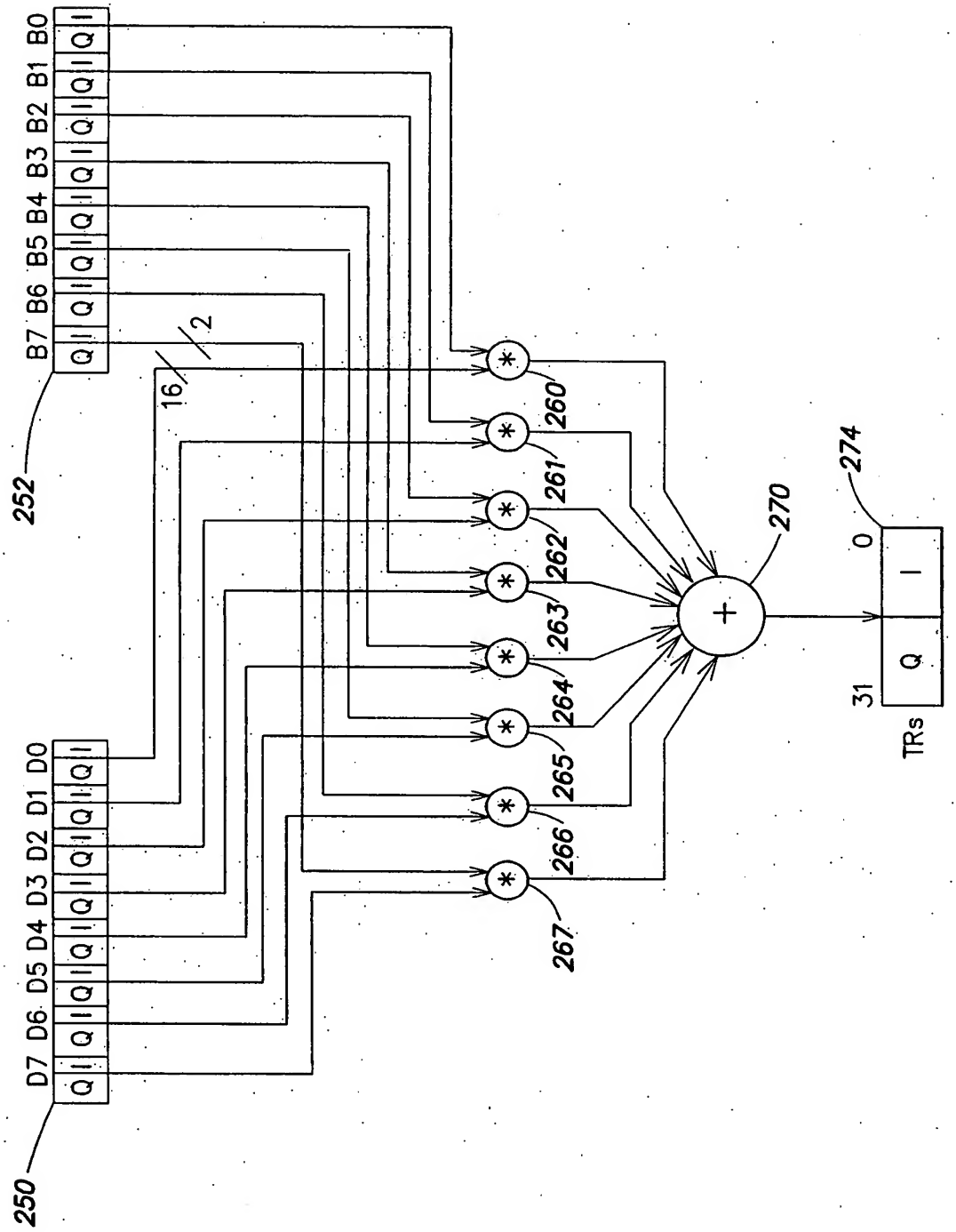
B0
B1
B2
B3
B4
B5
B6
B7
I
Q
252
16
2
D0
D1
D2
D3
D4
D5
D6
D7
250
260
261
262
263
264
265
266
267
270
274
0
31
TRs

FIG. 7

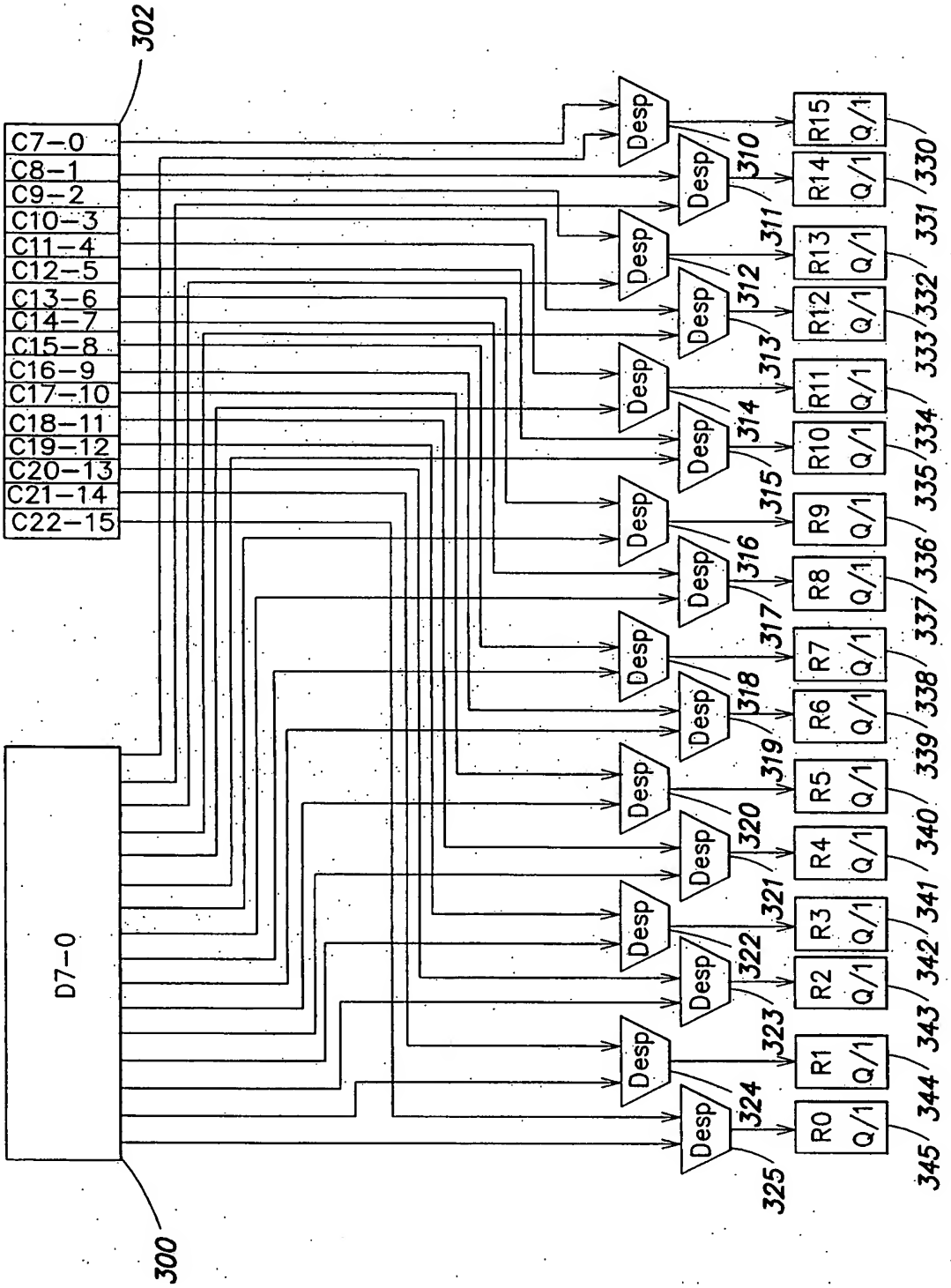
302
C7–0
C8–1
C9–2
C10–3
C11–4
C12–5
C13–6
C14–7
C15–8
C16–9
C17–10
C18–11
C19–12
C20–13
C21–14
C22–15
D7–0
300
Desp
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
R0
Q/1
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345

FIG. 8

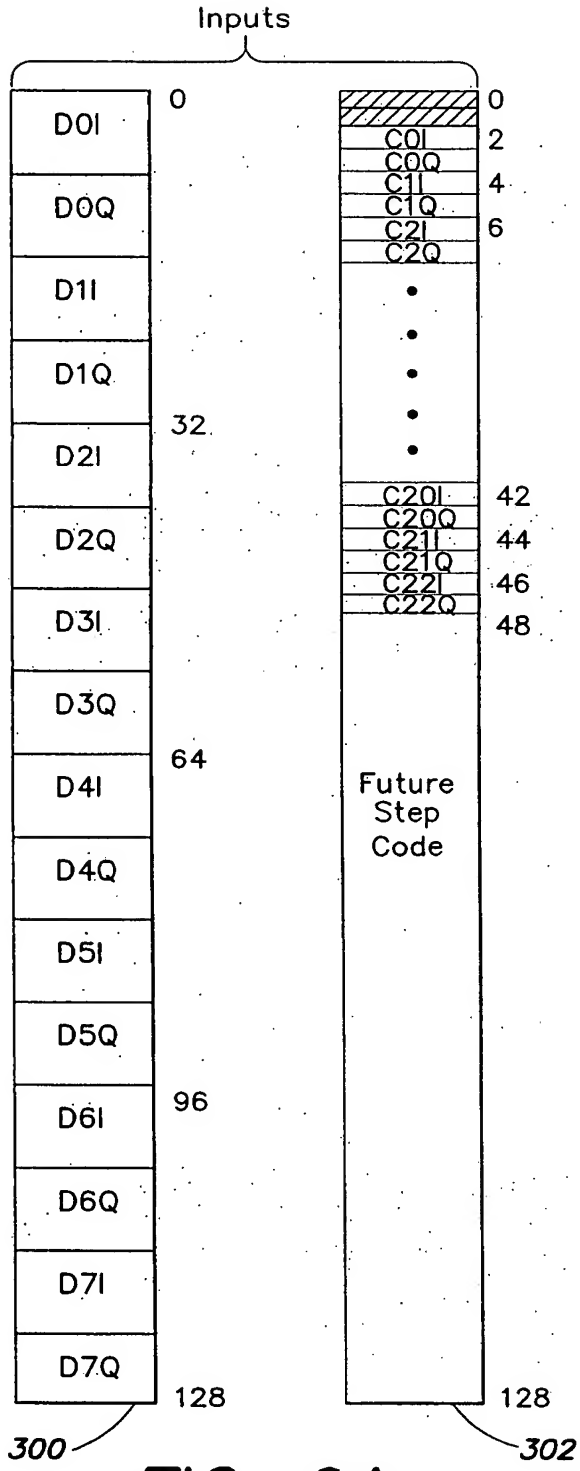
Inputs
D0I
D0Q
D1I
D1Q
D2I
D2Q
D3I
D3Q
D4I
D4Q
D5I
D5Q
D6I
D6Q
D7I
D7Q
0
32
64
96
128
300
C0I
C0Q
C1I
C1Q
C2I
C2Q
C20I
C20Q
C21I
C21Q
C22I
C22Q
0
2
4
6
42
44
46
48
Future Step Code
128
302

FIG. 9A

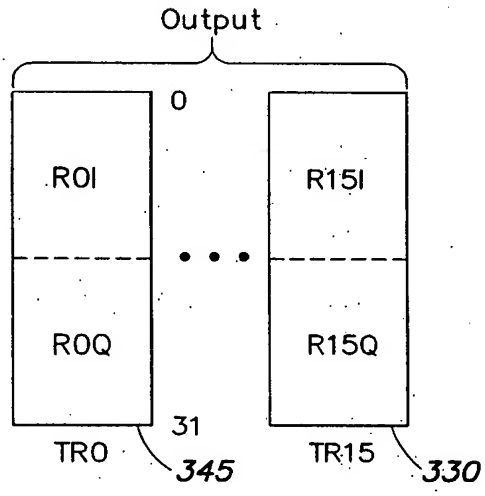
Output
R0I
R0Q
R15I
R15Q
0
31
TR0
TR15
345
330

FIG. 9B

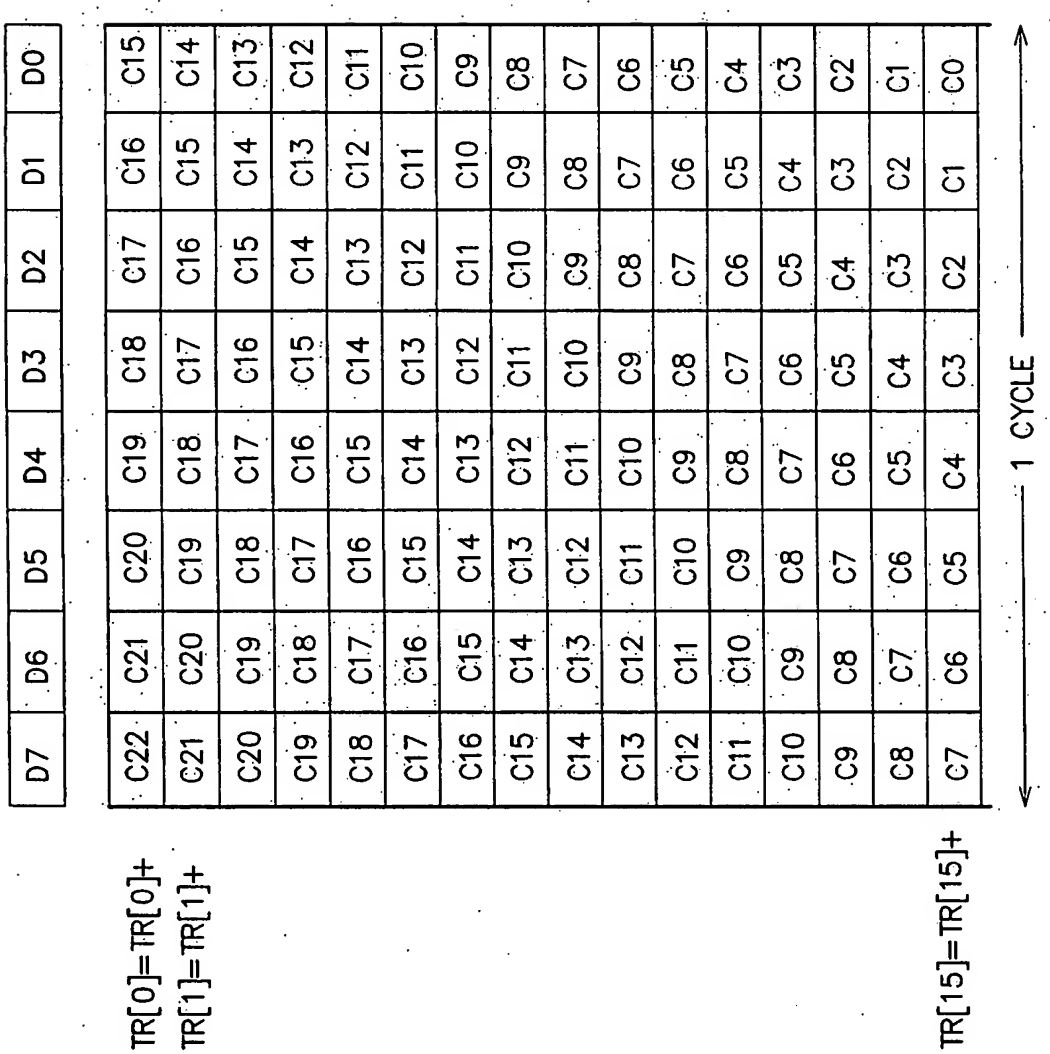
D7 D6 D5 D4 D3 D2 D1 D0
C22 C21 C20 C19 C18 C17 C16 C15
C21 C20 C19 C18 C17 C16 C15 C14
C20 C19 C18 C17 C16 C15 C14 C13
C19 C18 C17 C16 C15 C14 C13 C12
C18 C17 C16 C15 C14 C13 C12 C11
C17 C16 C15 C14 C13 C12 C11 C10
C16 C15 C14 C13 C12 C11 C10 C9
C15 C14 C13 C12 C11 C10 C9 C8
C14 C13 C12 C11 C10 C9 C8 C7
C13 C12 C11 C10 C9 C8 C7 C6
C12 C11 C10 C9 C8 C7 C6 C5
C11 C10 C9 C8 C7 C6 C5 C4
C10 C9 C8 C7 C6 C5 C4 C3
C9 C8 C7 C6 C5 C4 C3 C2
C8 C7 C6 C5 C4 C3 C2 C1
C7 C6 C5 C4 C3 C2 C1 C0
1 CYCLE
TR[0]= TR[0]+
TR[1]= TR[1]+
TR[15]= TR[15]+

FIG. 10

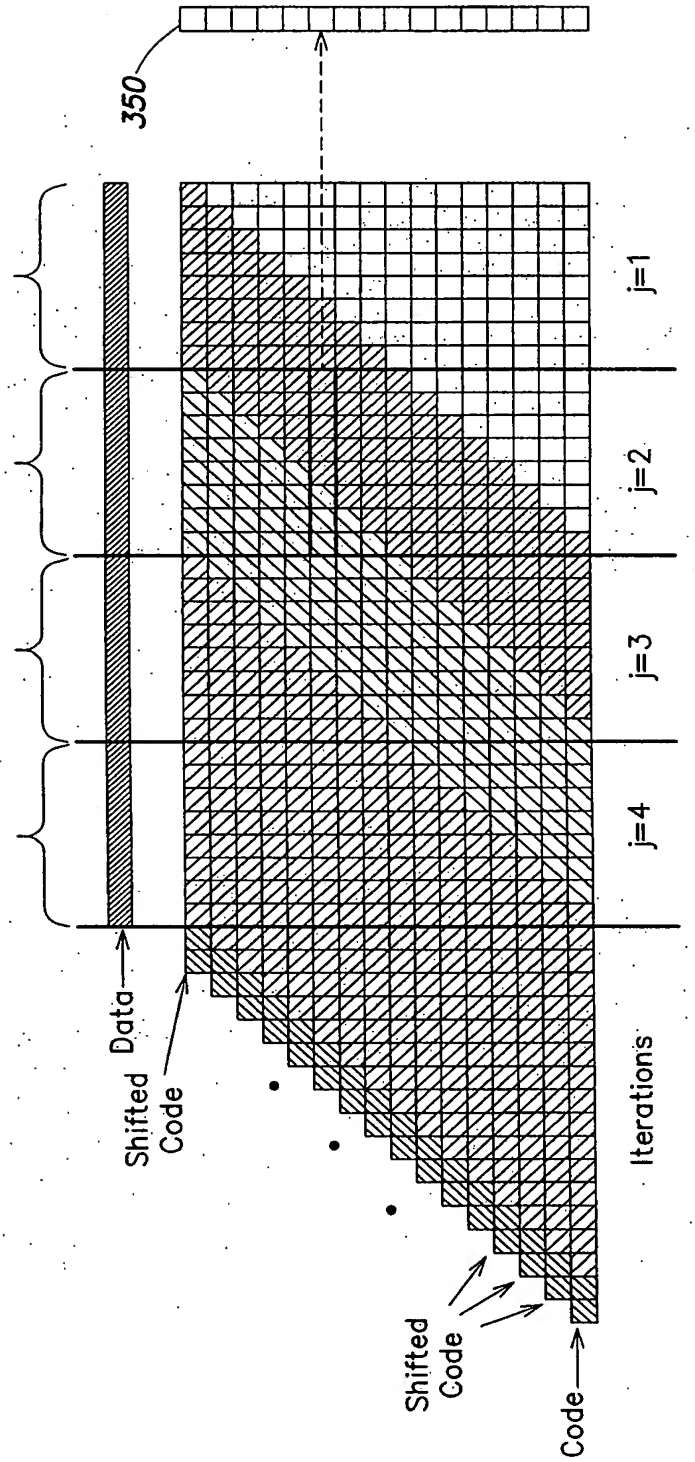
350
j=1
j=2
j=3
j=4
Data
Shifted Code
Iterations
Shifted Code
Code

FIG. 11